A Quasi-Static Optoelectronic ATM Switch

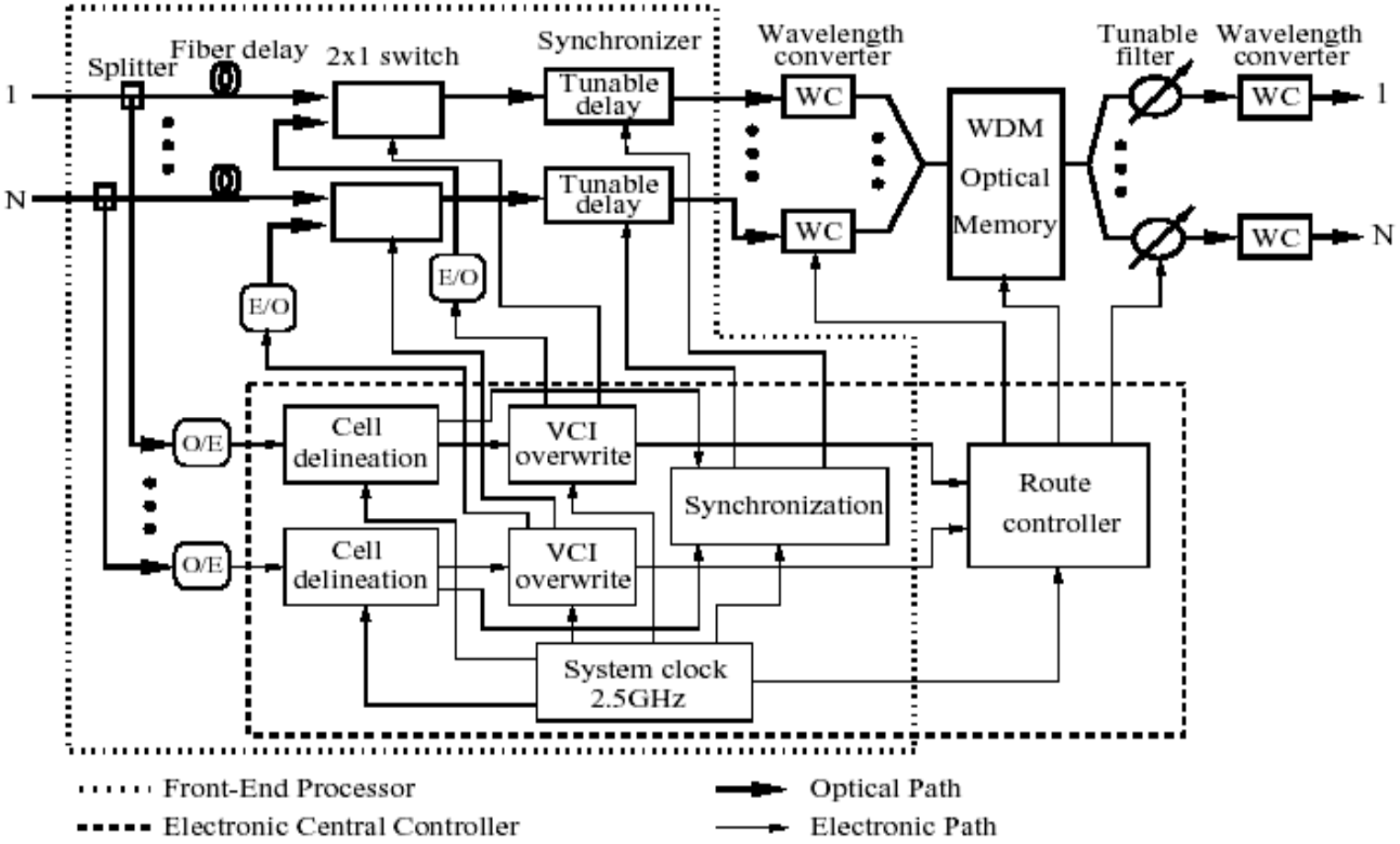
(NSF Grant 9814856)

Polytechnic University

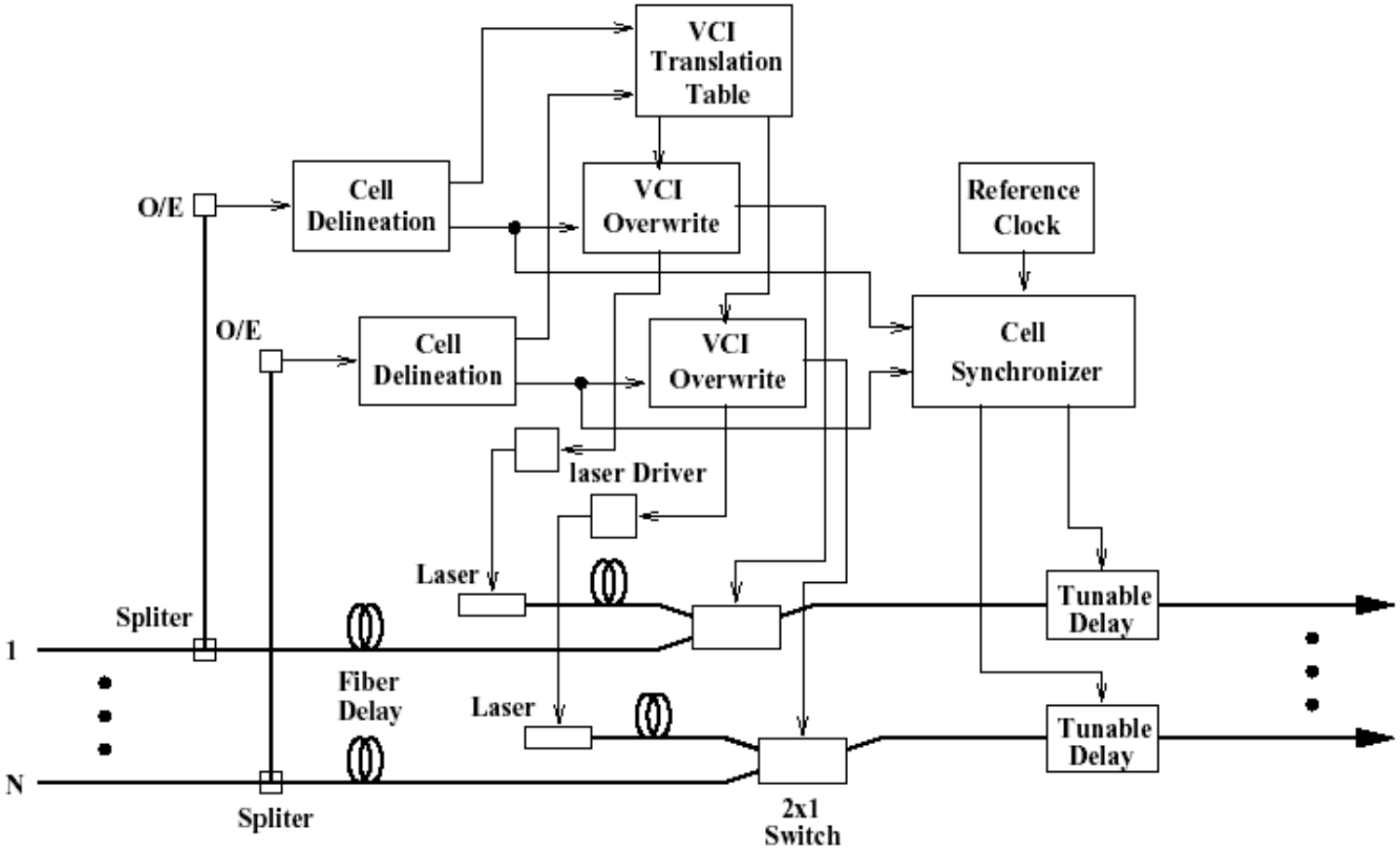
Project Objectives and Challenging Issues

- Objectives:
  - Based on the concept of the path switching, we propose a multi-terabit/s multicast ATM switch architecture that interconnects electronic switch modules with a quasi-static controlled optical interconnection network (OIN). Routing in the OIN is redetermined to avoid slot-by-slot processing and to provide flexible switching capacity on virtual path level. The surrounding electronic switch modules support multicasting, fast dynamic routing, and statistical multiplexing to compensate the quasi-static routing in the OIN to achieve totally a multi-terabit/s switching capacity. This quasi-static switching architecture simplifies the design of a multi-terabit/s ATM switch to specially featured 10 Gbit/s switch modules: the electronic multicast input and output modules and optical central interconnection, which are all feasible with existing technology.
  - We will investigate several approaches of performing output contention resolution within multicast electronic switch modules: determine a cost-effective design for each approach, study the performance in terms of throughput, cell delay and loss rate, and finally identify the best approach that has high performance and feasible construction complexity.

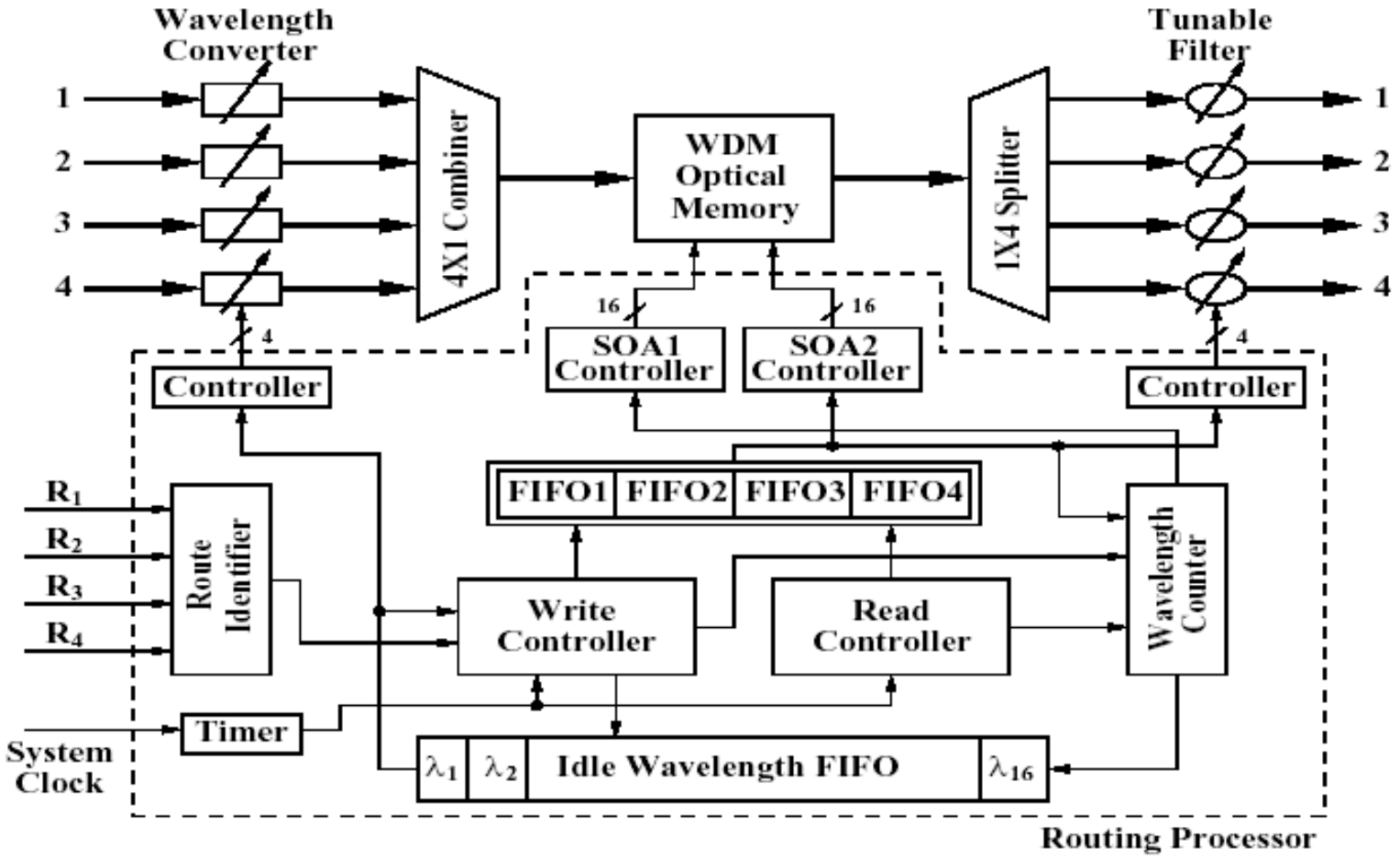
WDM-ATM Multicast (3M) Switch



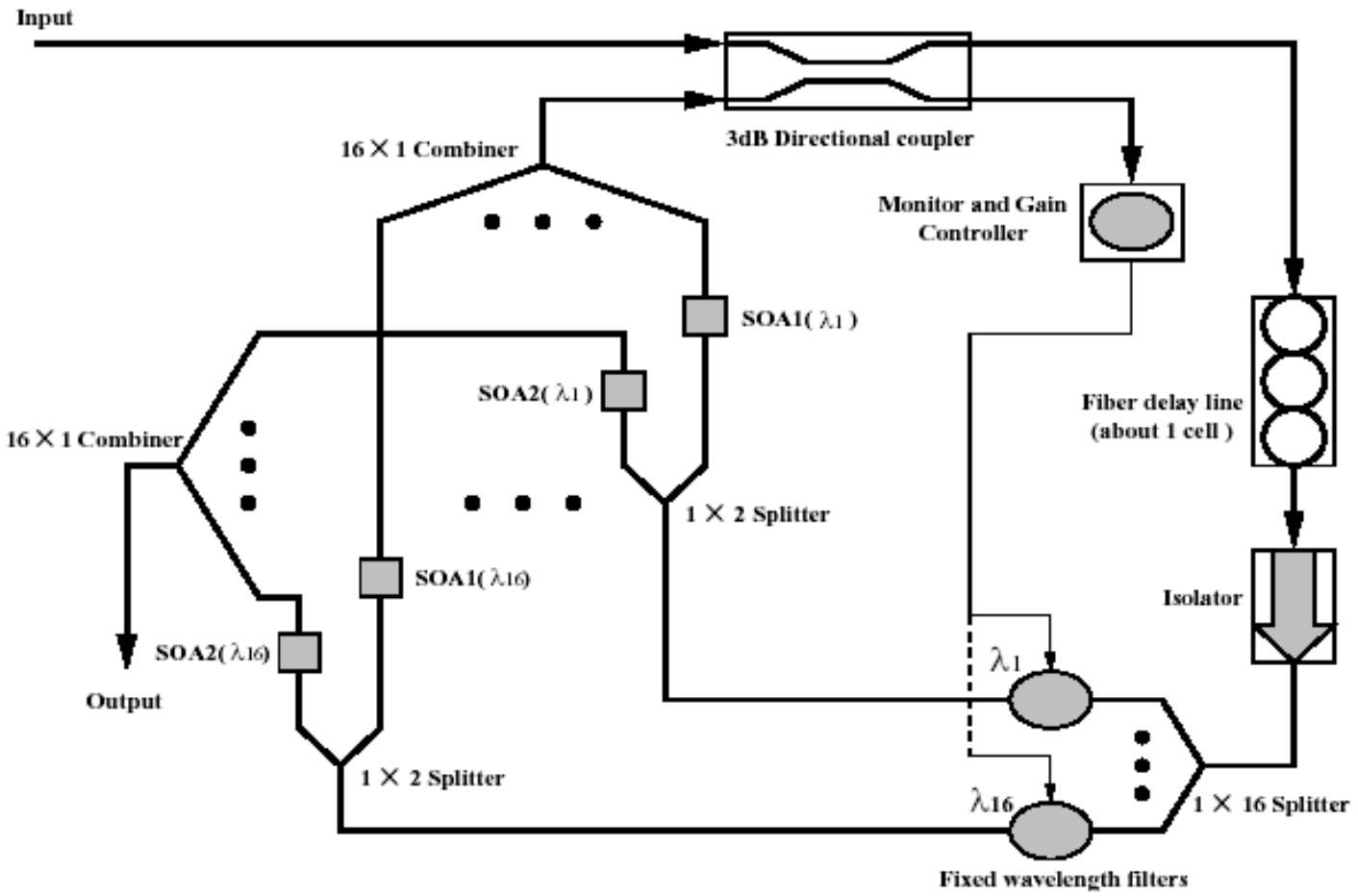
Photonic ATM Front-End Processor

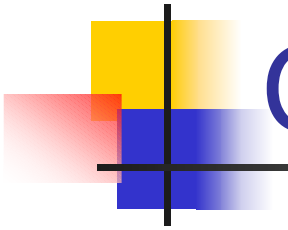


Optical Shared Memory Switch Fabric and Route Controller



WDM Loop Memory

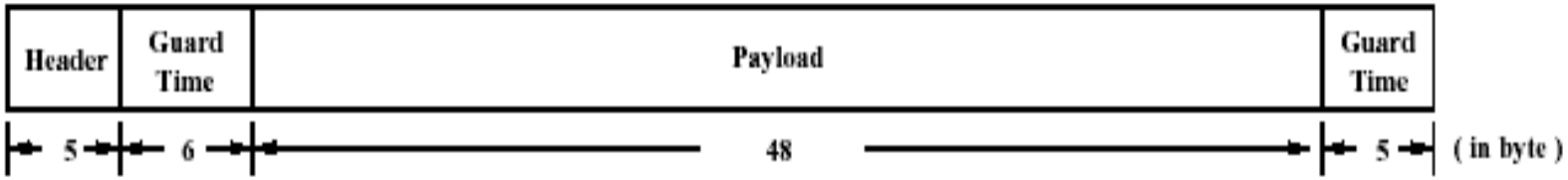




Cell Delineation Unit

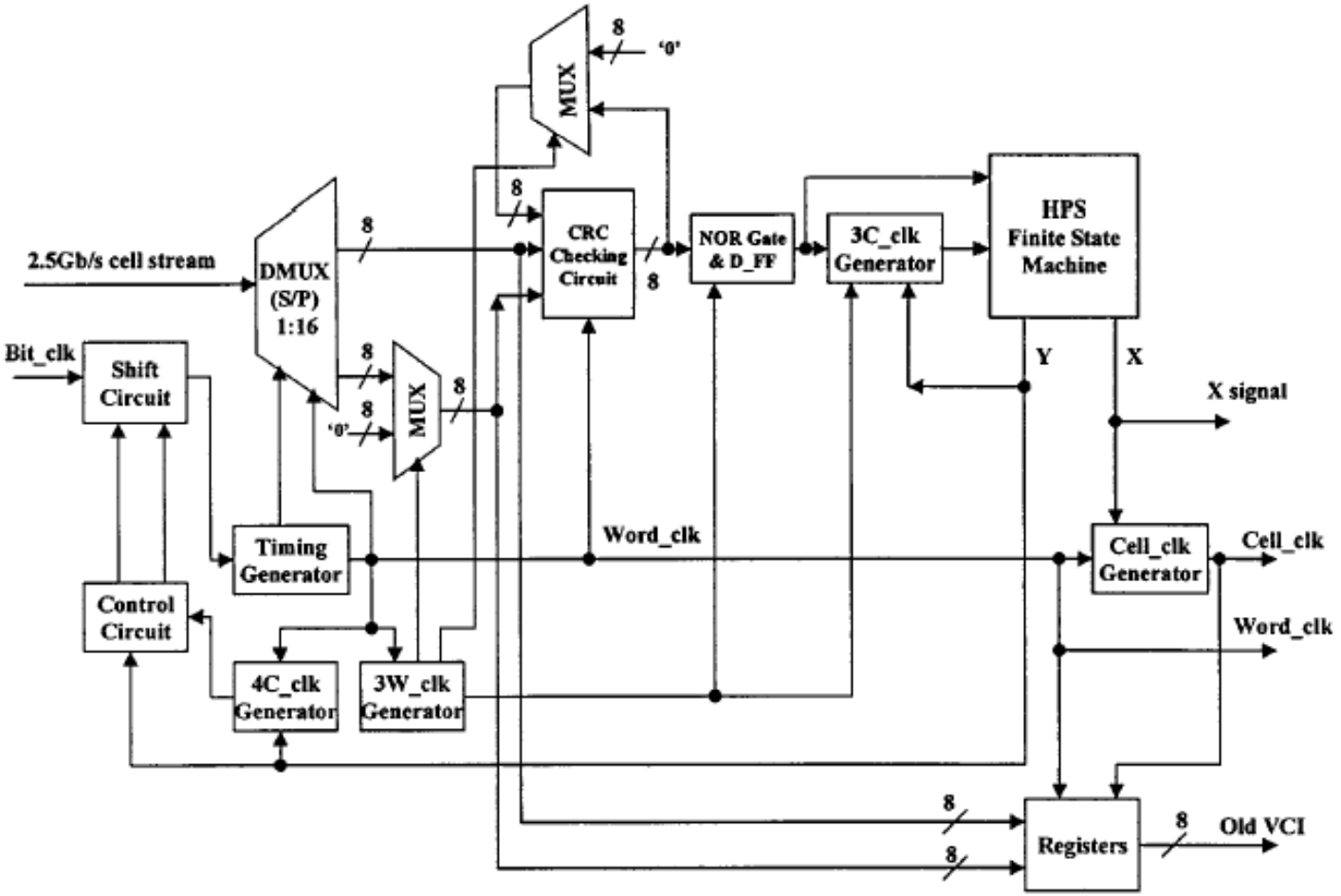
- Objective: Identify cell boundary
- Methods of cell delineation
  - The use of empty cells
    - It could take some time before the next empty cell will appear
  - The inserting of periodic cells
    - Trade off between repeating rate and fast confirmation
  - The inserting of simple pattern in every cell
    - Unreliable
  - The checking of the header error code (HEC)

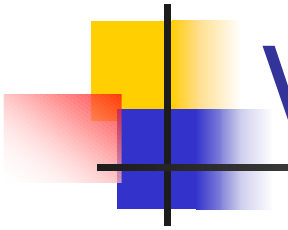
Cell Format



- Cells back to back, no SONET frame structure
- Cell length = 64 bytes, arbitrarily chosen for experiment
- Guard time : Time reserved for compensating slow response of optical devices

Block Diagram of Cell Delineation Unit

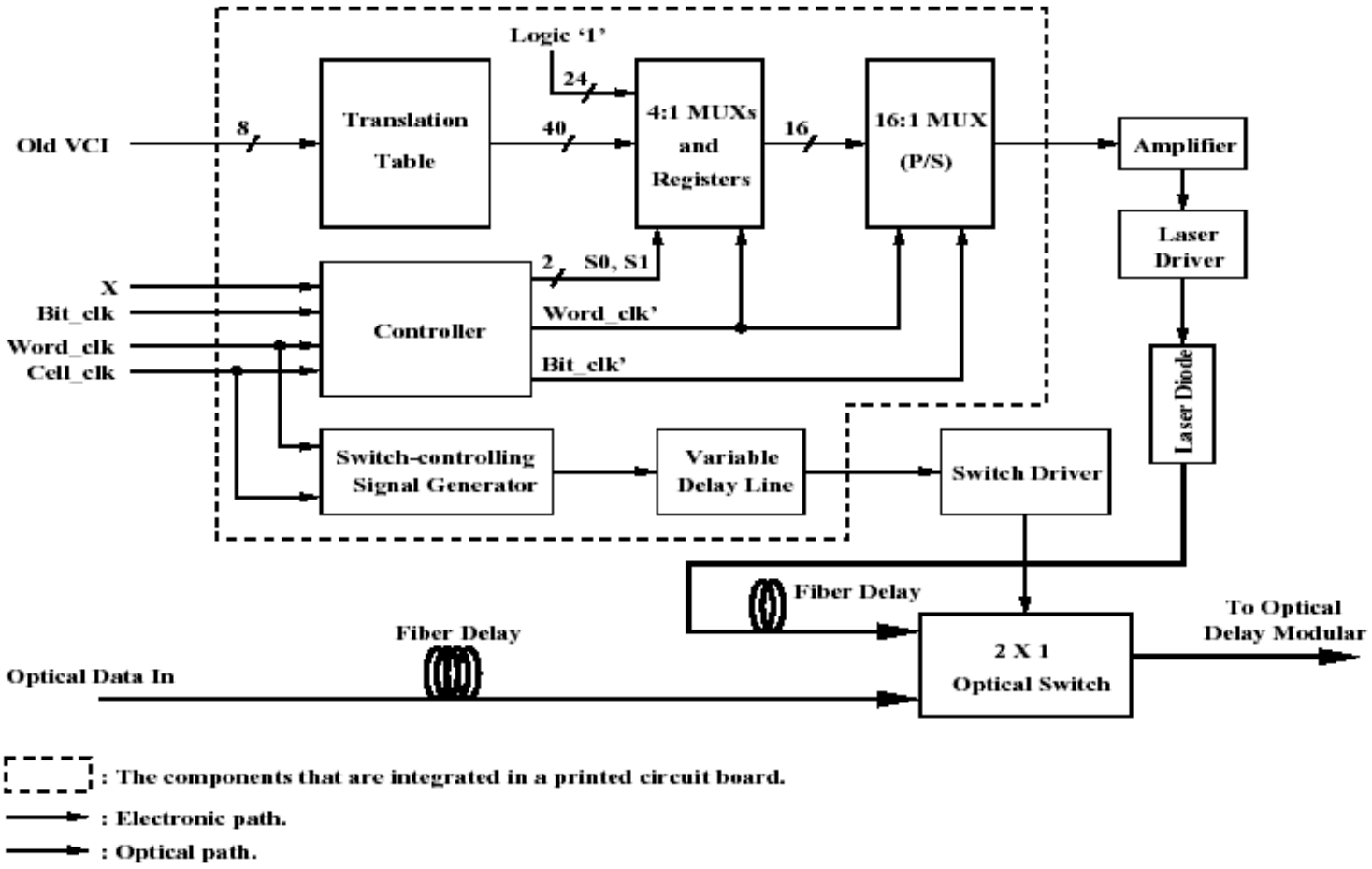




VCI Overwrite Unit

- Objective: Replace VPI/VCI and HEC bytes optically
- Key components and functions
  - VCI lookup table
    - Maintain new header data in the memory (EPROMs)
  - Parallel to serial converter
  - Switching-controlling signal generator
    - Generate a 6-bytes of pulse in every cell slot
    - Control on-off of optical switch
  - Optical devices
    - Laser driver and DFB Diode Laser
    - A 2x1 optical switch

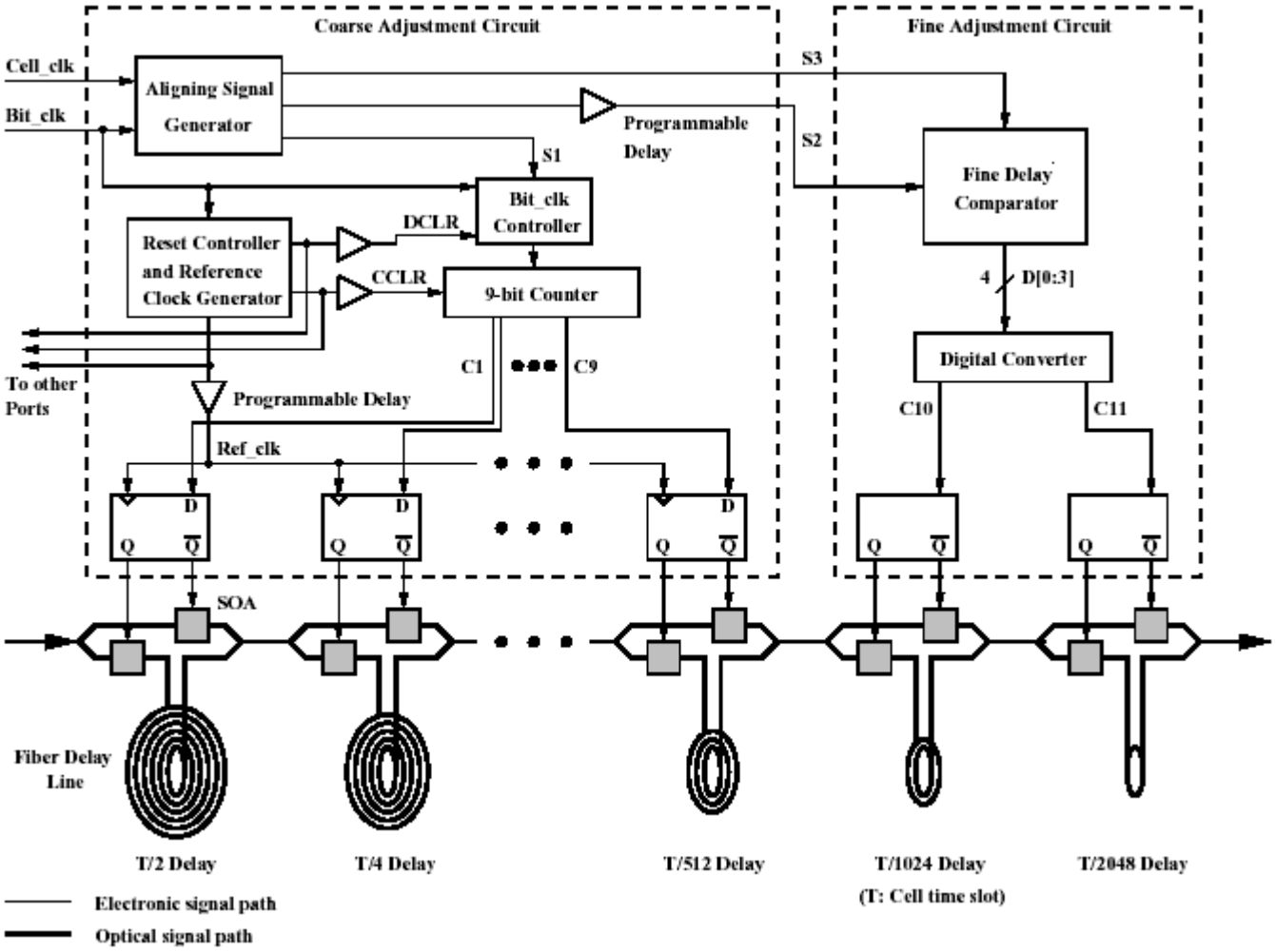
Block Diagram of VCI Overwrite Unit



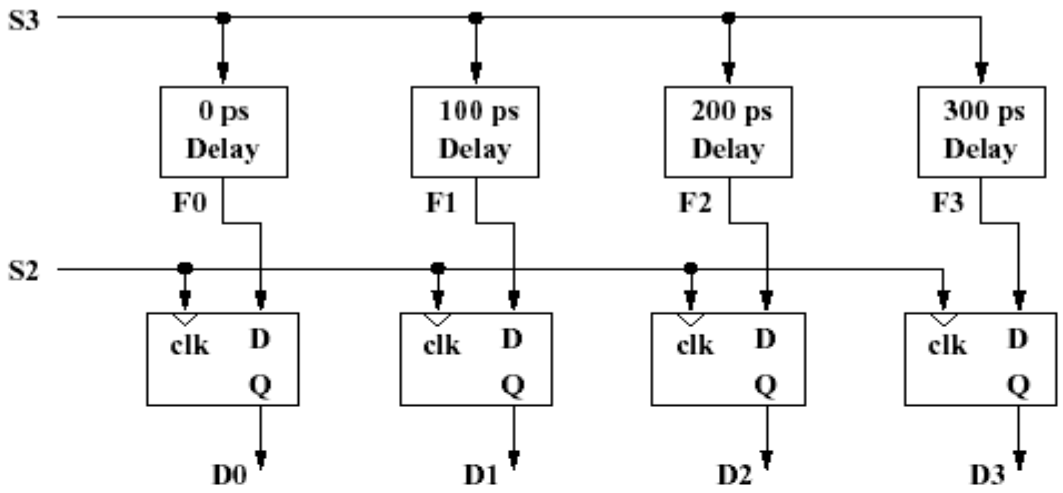
Cell Synchronization Unit

- Align optical ATM cells from different inputs to ¼bit resolution (100ps at 2.5 Gb/s line rate, or 2cm optical delay line)
- Align input cell streams to a reference cell clock
- Coarse synchronization circuit
  - Use a high-speed 9-bit counter to adjust the phase difference between 1 to 511 bits
- Fine synchronization circuit
  - Use sampling concept (each two samples apart by 100ps) to adjust the phase difference of 100, 200 or 300ps; i.e. ¼ ½ and ¾bit

Block Diagram of Cell Synchronization Unit



Fine Adjustment Circuit



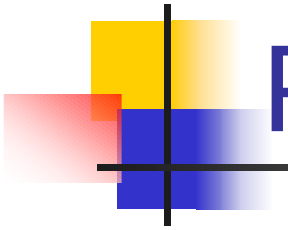
(a) Fine Delay Comparator

C10	C11	D0 (0ps)	D1 (100ps)	D2 (200ps)	D3 (300ps)
0	0	0	0	0	0
0	0	1	0	0	0
0	1	1	1	0	0
1	0	1	1	1	0
1	1	1	1	1	1

(b) Conversion table between [C10,C11] and [D0,D1,D2,D3]

Summary of Three PCB Characteristics

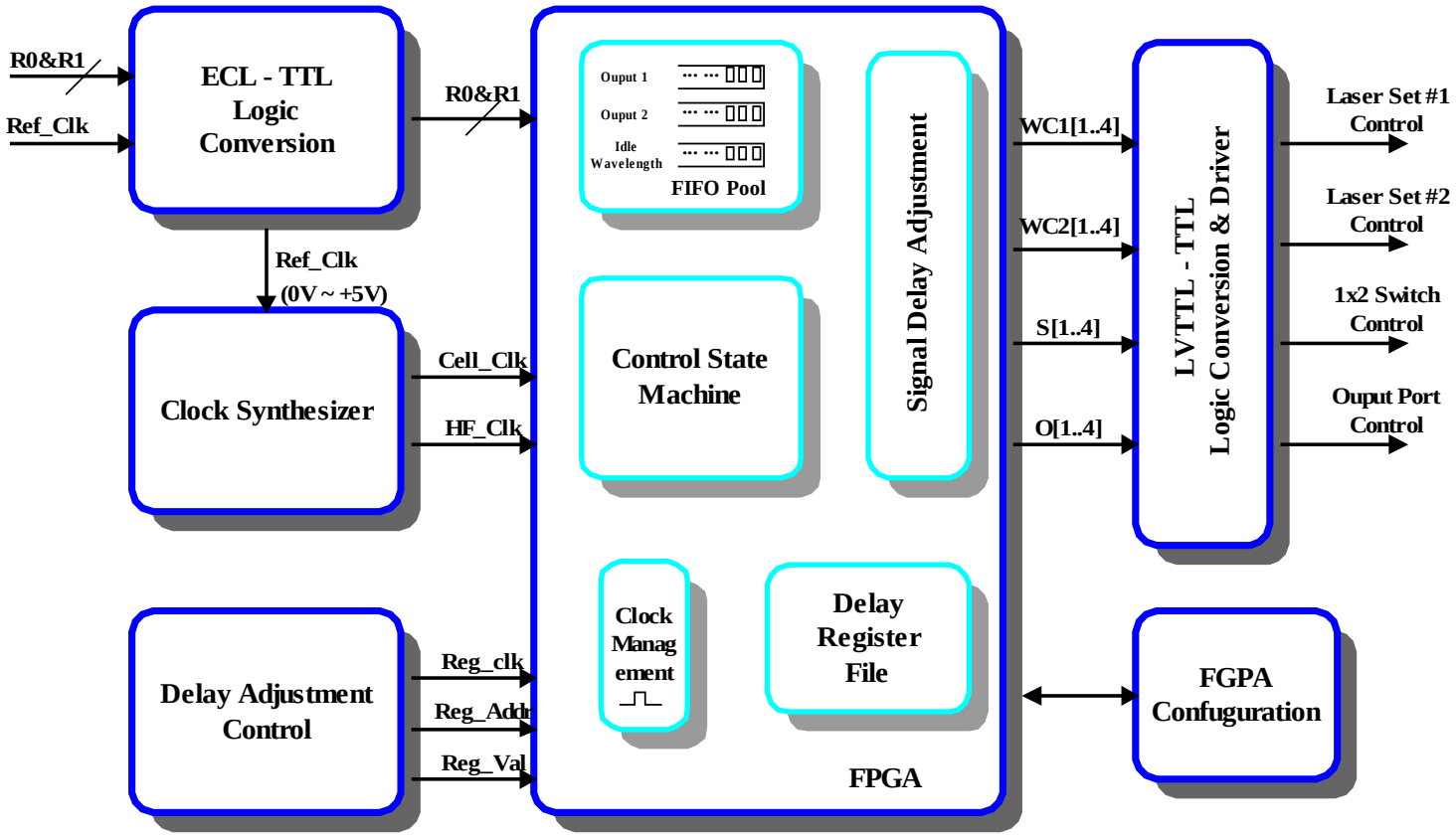
Board Name	Cell Delineation	VCI-Overwriting	Cell Synchronization
Size (inch)	15 x 13	15 x 10	15 x 20
Number of Layers	8	7	10
Material	Getek	Getek	Getek
Maximum Operation Speed	2.5 Gb/s	2.5 Gb/s	2.5 Gb/s
Power (watt)	40	25	41
Number of IC	95	94	61 + 36/N †
Components	Motorola's ECLinPS Family NEL GaAs IC NEL SST ECL Logic IC Vitesse's MUX/DMUX GaAs IC Atmel's AT27C256R EPROM		



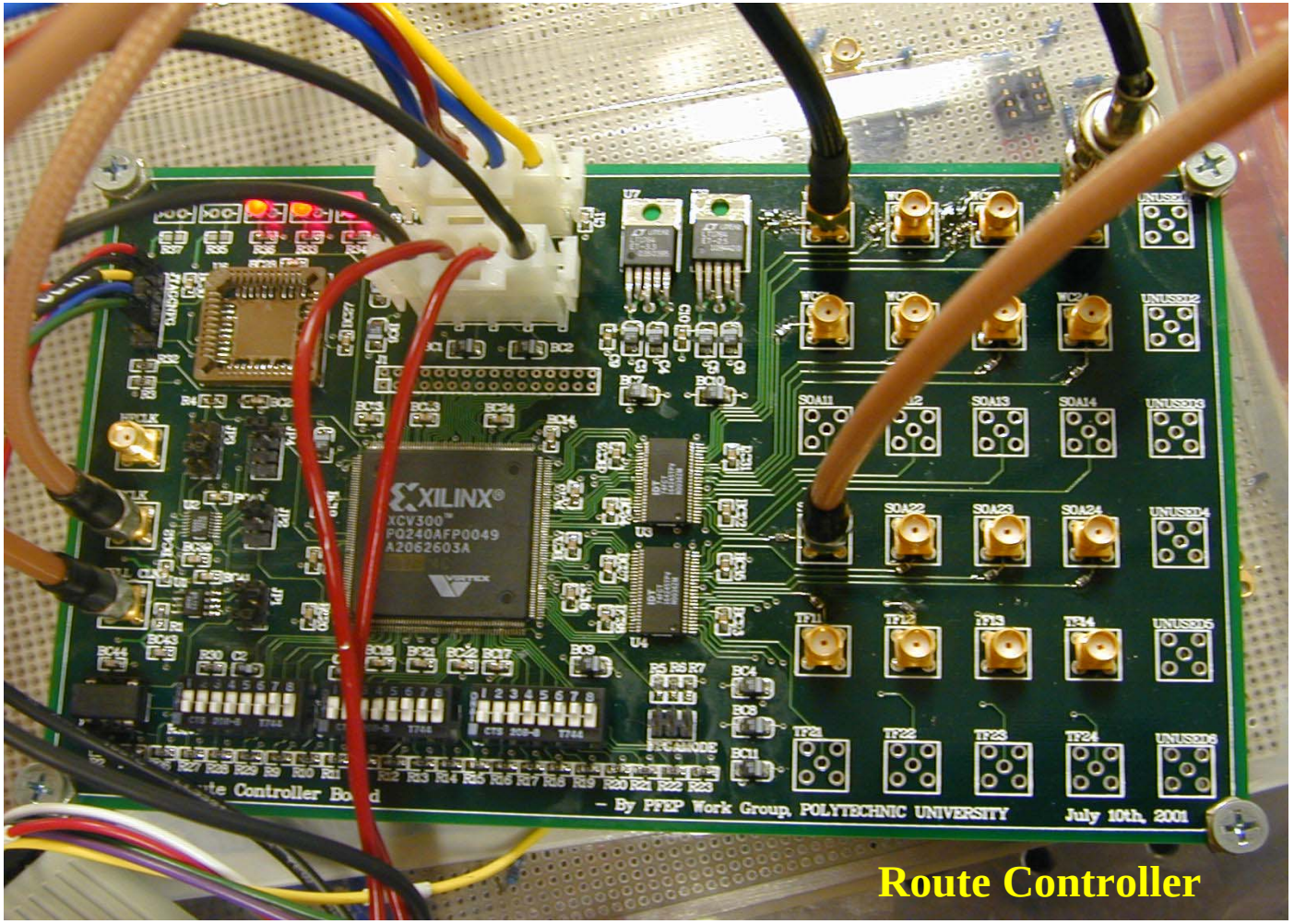
Route Controller Unit

- Objective: Control the loop memory for cell switching
- Methods of switching control:
  - Treat wavelengths as memory units, then it behaves like a shared memory switch
  - Maintaining two FIFOs to store wavelength IDs destined for each output port respectively
  - Maintaining one FIFO to store idle wavelength IDs that can be allocated to input cells
  - Wavelength IDs pulled out from output FIFOs are recycled back to idle wavelength FIFO for future use.

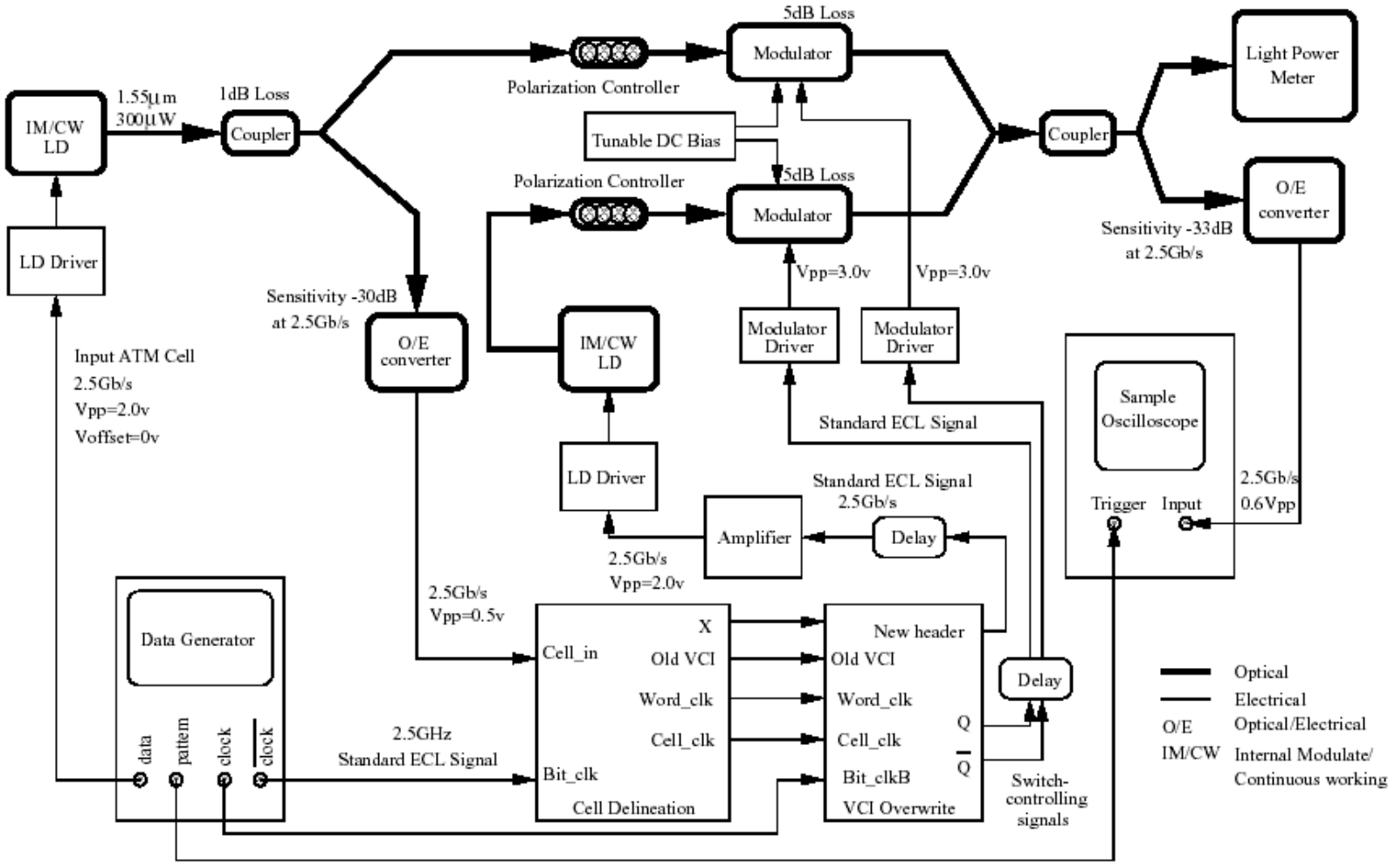
Route Controller Block Diagram



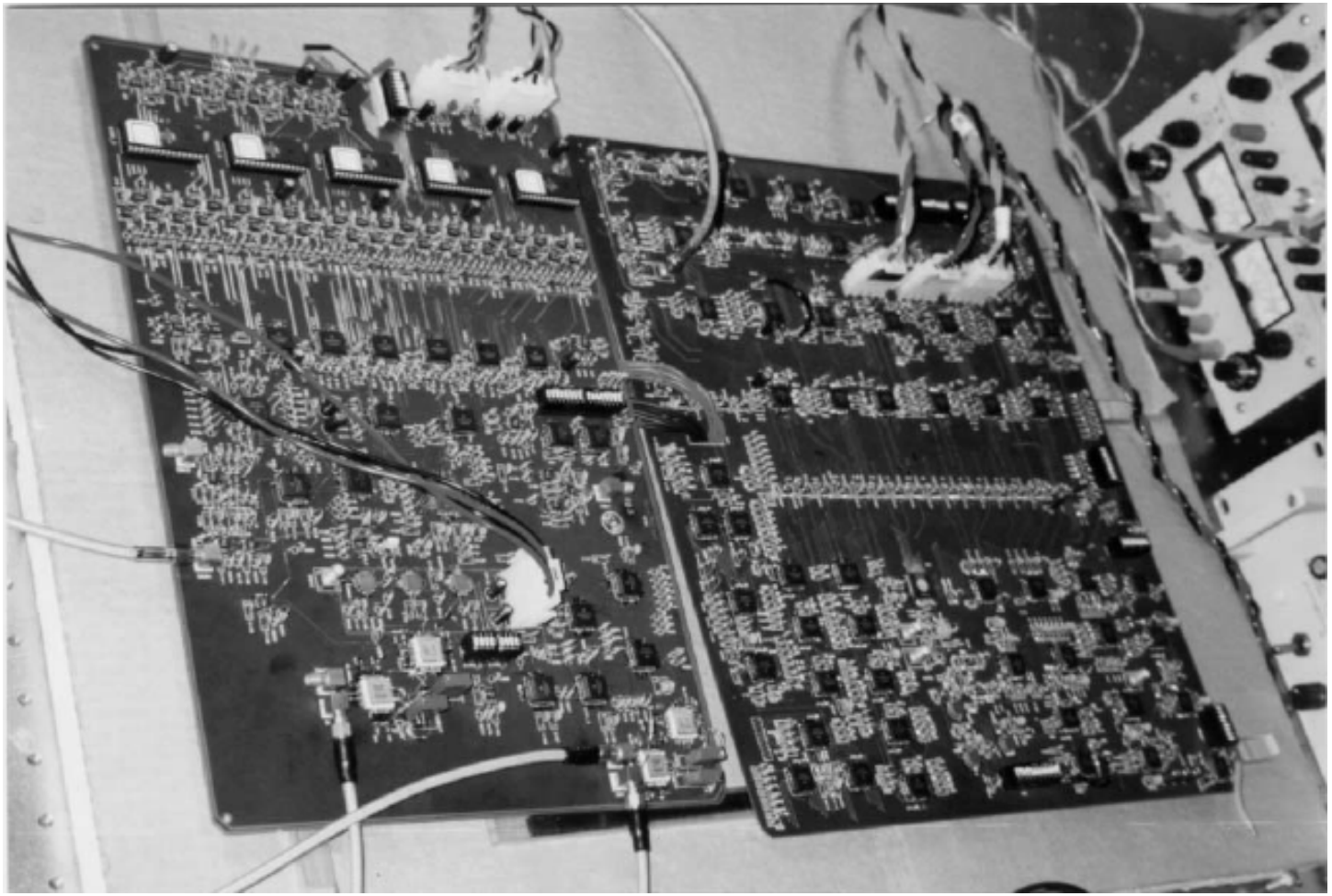
Route Controller Board Picture



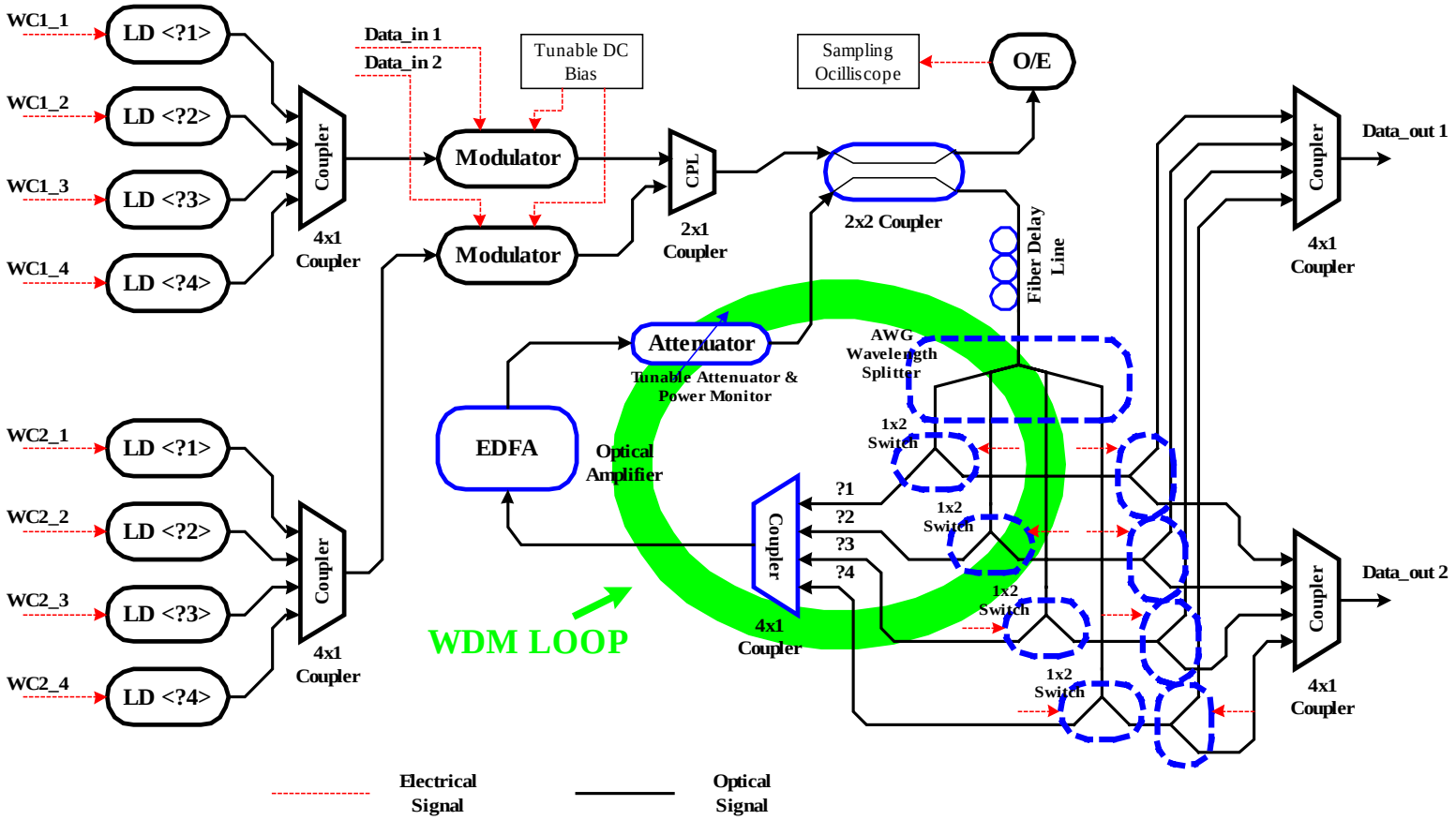
Testing Setup of Cell Delineation & VCI Overwrite Units



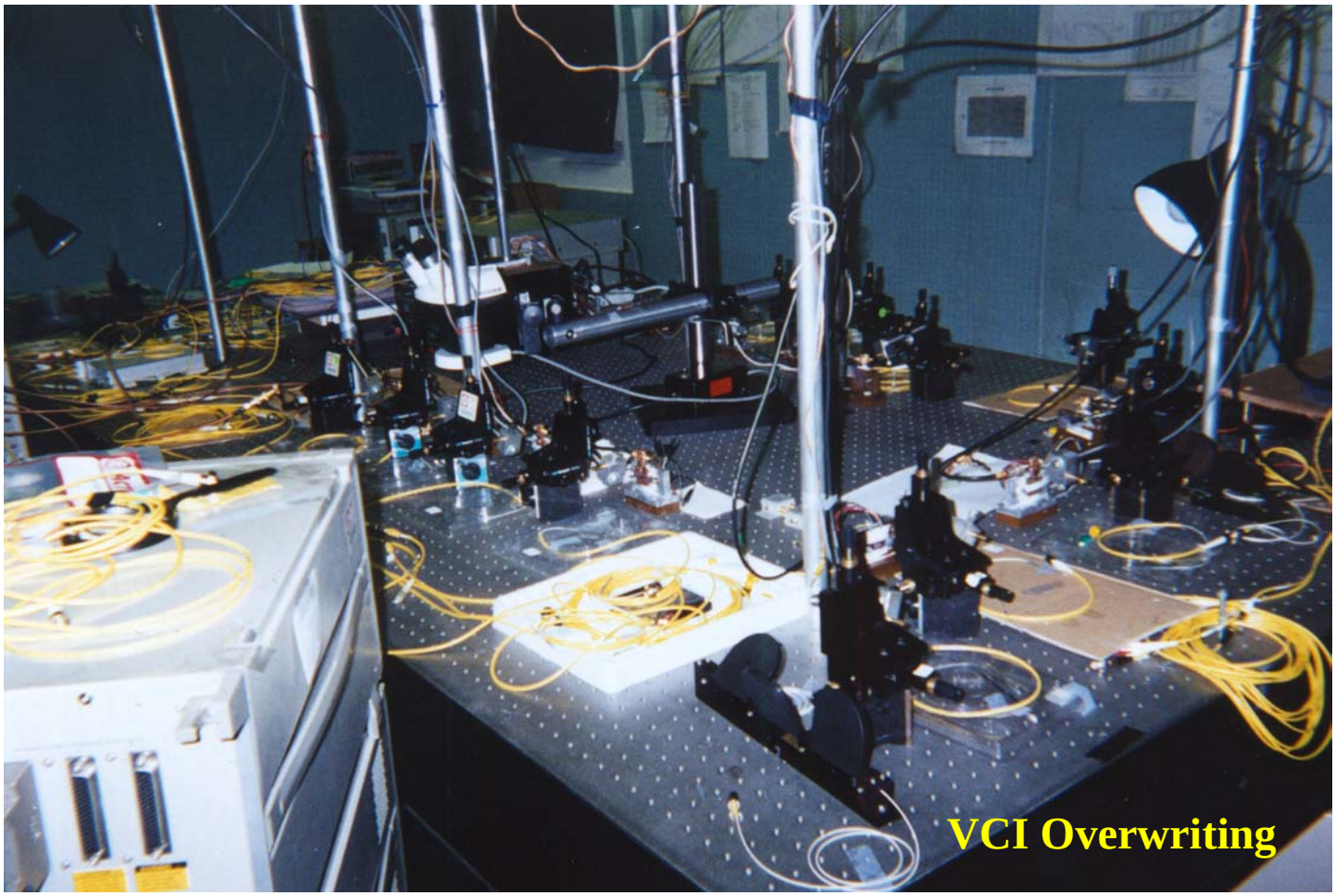
Cell Delineation & VCI Overwrite Units Setup Picture



Optical Setup for 2x2 Loop Switch



Optical Setup Picture I



Optical Setup Picture II

Optical Setup Picture III